

SECTION VIII SERVICE

8-1. INTRODUCTION

8-2. This section provides safety considerations, logic symbols, troubleshooting procedures, block diagram and description, circuit theory, component location photos, and schematic diagram (service information).

8-3. SAFETY CONSIDERATIONS

8-4. Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to retain the instrument in safe condition (see Sections II, III, and V). Service and adjustments should be performed only by qualified service personnel.

WARNING

ANY INTERRUPTION OF THE PROTECTIVE (GROUNDING) CONDUCTOR (INSIDE OR OUTSIDE THE INSTRUMENT) OR DISSECTION OF THE PROTECTIVE EARTH TERMINAL IS LIKELY TO MAKE THE INSTRUMENT DANGEROUS. INTENTIONAL INTERRUPTION IS PROHIBITED.

8-5. Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

8-6. Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

8-7. Make sure that only fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement. The use of repaired fuses and the short-circuiting of fuseholders must be avoided.

8-8. Whenever it is likely that this protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

WARNING

THE SERVICE INFORMATION IS OFTEN USED WITH LINE POWER SUPPLIED AND PROTECTIVE COVERS REMOVED FROM THE INSTRUMENT. ENERGY AVAILABLE AT MANY POINTS MAY, IF CONTACTED, RESULT IN PERSONAL INJURY.

8-9. RECOMMENDED TEST EQUIPMENT

8-10. Test equipment and test equipment accessories required to maintain the 5004A are listed in *Table 7-2*. Equipment other than that listed may be used if it meets the listed critical specifications.

8-11. LOGIC SYMBOLS

8-12. Logic symbols used in this manual conform to the American National Standard ANSI Y32.14-1973 (IEE Std. 91-1973). This standard supersedes MIL-STD-806B. In the following paragraphs logic symbols are described.

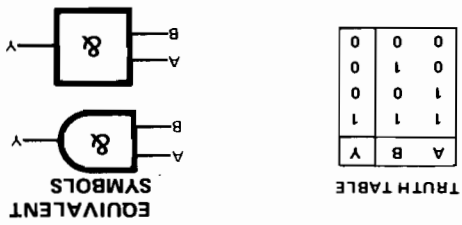
8-13. Logic Concepts

8-14. The binary numbers 1 and 0 are used in pure logic where 1 represents true, yes, or active and 0 represents false, no, or inactive. These terms should not be confused with the physical quantity (e.g., voltage) that may be used to implement the logic, nor should the term "active" be confused with a level that turns a device on or off. A truth table for a relationship in logic shows (implicitly or explicitly) all the combinations of true and false input conditions and the result (output). There are only two basic logic relationships, AND and OR. The following illustrations assume two inputs (A and B), but these can be generalized to apply to more than two inputs.

AND Y is true if and only if A is true and B is true (or more generally, if all inputs are true).

$$Y = A \bullet B$$

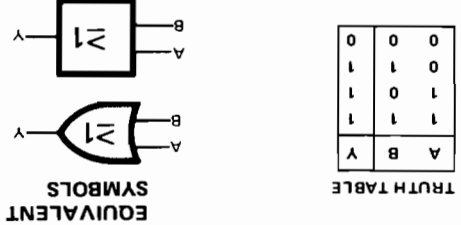
Y=1 if and only if A=1 and B=1.



OR Y is true if and only if A is true or B is true (or more generally, if one or more input(s) is (are) true).

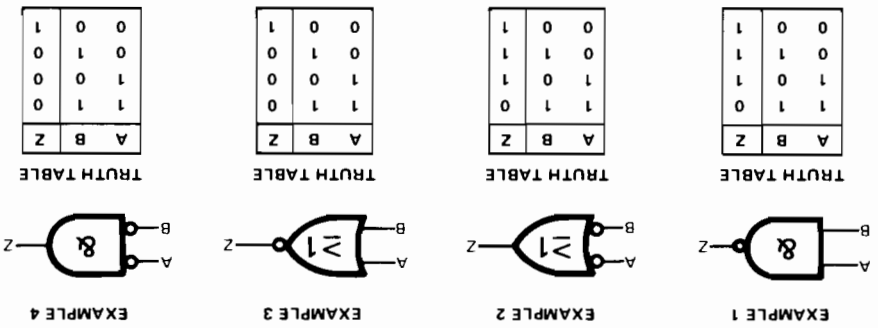
Y=1 if and only if A=1 or B=1.

$$Y = A + B$$



8-15. Negation

8-16. In logic symbology, the presence of the negation indication symbol 0 provides for the representation of logic function inputs and outputs in terms independent of their physical values; the 0-state of the input or output being the 1-state of the symbol referred to by the symbol description.



EXAMPLE 1 says that Z is not true if A is true and B is true or that Z is true if A and B are not both true. $Z = AB$ or $Z = \overline{A+B}$. This is frequently referred to as NAND (for NOT AND). EXAMPLE 2 says that Z is true if A is not true or if B is not true. $Z = A + B$. Note that this truth table is identical to that of Example 1. The logic equation is merely a De Morgan's transformation of the equations in Example 1. The symbols are equivalent.

EXAMPLE 3 $Z = A + B$ or $Z = \overline{A \cdot B}$ and,

EXAMPLE 4 $Z = A \cdot B$, also share common truth table and are equivalent transformations of each other. The NOT OR form (Example 3) is frequently referred to as NOR.

NOTE

In this manual the logic negation symbol is NOT used.

8-17. Logic Implementation and Polarity Indication

8-18. Devices that can perform the basic logic functions, AND and OR, are called gates. Any device that can perform one of these functions can also be used to perform the other if the relationship of the input and output voltage levels to the logic variables 1 and 0 is redefined suitably.

8-19. In describing the operation of electronic logic devices, the symbol H is used to represent a "high level," which is a voltage within the more-positive (less-negative) of the two ranges of voltages used to represent the binary variables. L is used to represent a "low level," which is a voltage within the less-positive (more-negative) range.

8-20. A function table for a device shows (implicitly or explicitly) all the combinations of input conditions and the resulting output conditions.

8-21. In graphic symbols, inputs or outputs that are active when at the high level are shown without polarity indication. The polarity indicator symbol ∇ denotes that the active (one) state of an input or output with respect to the symbol to which it is attached is the low level.

NOTE

The polarity indicator symbol " ∇ " is used in this manual.

EXAMPLE 5

Assume two devices having the following function tables.

DEVICE #1	
A	B
L	L
L	H
H	L
H	H
FUNCTION TABLE	

DEVICE #2	
A	B
L	L
L	H
H	L
H	H
FUNCTION TABLE	

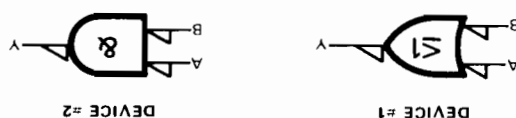
POSITIVE LOGIC

By assigning the relationships $H=1$, $L=0$ at both input and output, Device #1 can perform the AND function and Device #2 can perform the OR function. Such a consistent assignment is referred to as positive logic. The corresponding logic symbols would be:



NEGATIVE LOGIC

Alternatively, by assigning the relationship $H=0$, $L=1$ at both input and output, Device #1 can perform the OR function and Device #2 can perform the AND function. Such a consistent assignment is referred to as negative logic. The corresponding logic symbols would be:



8-22. MIXED LOGIC. The use of the polarity indicator symbol (∇) automatically invokes a mixed-logic convention. This is, positive logic is used at the input and outputs that do not have polarity indicators, negative logic is used at the inputs and outputs that have polarity indicators.

EXAMPLE 6

A	B	Z
H	H	L
H	L	H
L	H	H
L	L	L

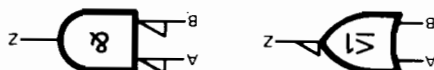
This may be shown either of two ways:



EXAMPLE 7

A	B	Z
H	H	L
H	L	L
L	H	L
L	L	L

This may be shown either of two ways:



Note the equivalence of these symbols to examples 1 and 2 and the fact that the function table is a positive-logic translation ($H=1$, $L=0$) of the NAND truth table, and also note that the function table is a positive-logic translation ($H=1$, $L=0$) of the NOR truth table, and also note that the function table is the negative-logic translation ($H=0$, $L=1$) of the NAND truth table, given in Example 1.

8-23. It should be noted that one can easily convert from the symbology of positive-logic merely by substituting a polarity indicator (∇) for each negative indicator (\circ) while leaving the distinctive shapes alone. To convert from the symbology of negative logic, a polarity indicator (∇) is substituted for each negative indicator (\circ) and the OR shape is substituted for the AND shape or vice versa.

8-24. It was shown that any device that can perform OR logic can also perform AND logic and vice versa. De Morgan's transformation is illustrated in Examples 1 through 7. The rules of the transformation are:

1. At each input or output having a negation (\circ) or polarity (∇) indicator, delete the indicator.
2. At each input or output not having an indicator, add a negation (\circ) or polarity (∇) indicator.
3. Substitute the AND symbol (\square) for the OR symbol (∇) or vice versa.

These steps do not alter the assumed convention; positive-logic stays positive, negative-logic stays negative, and mixed-logic stays mixed.

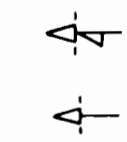
8-25. The choice of symbol may be influenced by these considerations: (1) The operation being performed may best be understood as AND or OR. (2) In a function more complex than a basic gate, the inputs will usually be considered as inherently active high or active low (e.g., the j and k inputs of a J-K flip-flop are active high and active low, respectively). (3) In a chain of logic, understanding and the writing of logic equations are often facilitated if active-low or negated outputs feed into active-low or negated inputs.

8-26. Other Symbols

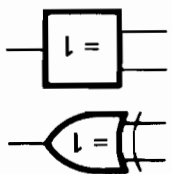
8-27. More symbols are required to depict complex logic diagrams. Some of the other symbols are as follows:

Dynamic input activated by transition from a low level to a high level. The opposite transition has no effect at the output.

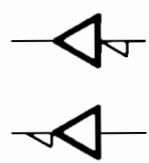
Dynamic input activated by transition from a high level to a low level. The opposite transition has no effect at the output.



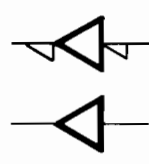
Exclusive OR function. The output will assume its indicated active level if and only if one and only one of the two inputs assumes its indicated active level.



Inverting function. The output is low if the input is high and it is high if the input is low. The two symbols shown are equivalent.



Noninverting function. The output is high if the input is high and it is low if the input is low. The two symbols shown are equivalent.



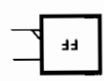
OUTPUT DELAY. The output signal is effective when the input signal returns to its opposite state.



EXTENDER. Indicates when a logic function increases (extends) the number of inputs to another logic function.



FLIP-FLOP. A binary sequential element with two stable states: a set (1) state and a reset (0) state. Outputs are shown in the 1 state when the flip-flop is set. In the reset state the outputs will be opposite to the set state.



RESET. A 1 input will reset the flip-flop. A return to 0 will cause no further effect.



SET. A 1 input will set the flip-flop. A return to 0 will cause no further action.



TOGGLE. A 1 input will cause the flip-flop to change state. A return to 0 will cause no further action.



J INPUT. Similar to the S input except if both J and K (see below) are at 1, the flip-flop changes state.

K INPUT. Similar to the R input (see above).

D INPUT (Data). Always dependent on another input (usually C). When the C and D inputs are at 1, the flip-flop will be set. When the C is 1 and the D is 0, the flip-flop will reset.



Address symbol has multiplexing relationship at inputs and demultiplexing relationship at outputs.

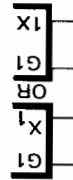
8-28. Dependency Notation "C" "G" "V" "F"

8-29. Dependency Notation is a way to simplify symbols for complex IC elements by defining the existence of an AND relationship between inputs, or by the AND conditioning of an output by an input without actually showing all the elements and interconnections involved. The following examples use the letter "C" for control and "G" for gate. The dependent input is labeled with a number that is either prefixed (e.g., 1X) or subscripted (e.g., X₁). They both mean the same thing. The letter V is used to indicate an OR relationship between inputs or between inputs and outputs with this letter (V). The letter F indicates a connect-disconnect relationship. If the F (free dependency) inputs or outputs are active (1) the other usual normal conditions apply. If one or more of the F inputs are inactive (0), the related F output is disconnected from its normal output condition (it floats).

The input that controls or gates other inputs is labeled with a "C" or a "G", followed by an identifying number. The controlled or gated input or output is labeled with the same number. In this example, "1" is controlled by "G1."



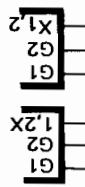
When the controlled or gated input or output already has a functional label (X is used here), that label will be prefixed or subscripted by the identifying number.



If a particular device has only one gating or control input then the identifying number may be eliminated and the relationship shown with a subscript.



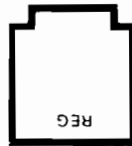
If the input or output is affected by more than one gate or control input, then the identifying numbers of each gate or control input will appear in the prefix or subscript, separated by commas. In this example "X" is controlled by "G1" and "G2."



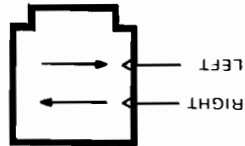
8-30. Control Blocks

8-31. A class of symbols for complex logic are called control blocks. Control blocks are used to show where common control signals are applied to a group of functionally separate units. Examples of types of control blocks follow.

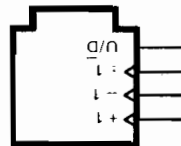
Register control block. This symbol is used with an associated array of flip-flop symbols to provide a point of placement for common function lines, such as a common clear.



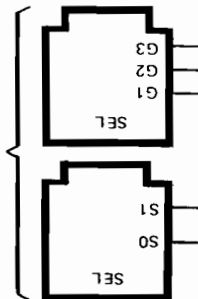
Shift register control block. These symbols are used with any array of flip-flop symbols to form a shift register. An active transition at the inputs causes left or right shifting as indicated.



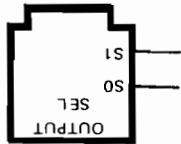
Counter control block. The symbol is used with an array of flip-flops or other circuits serving as a binary or decade counter. An active transition at the +1 or -1 input causes the counter to increment one count upward or downward, respectively. An active transition at the ± 1 input causes the counter to increment one count upward or downward depending on the input at an up/down control.



Selector control block. These symbols are used with an array of OR symbols to provide a point of placement for selection (S) or gating (G) lines. The selection lines enable the input designated 0, 1, ..., n of each OR function by means of a binary code where S0 is the least-significant digit. If the 1 level of these lines is low, polarity indicators (∇) will be used. The gating lines have an AND relation with the respective input of each OR function: G1 with the inputs numbered 1, G2 with the input numbered 2, and so forth. If the enabling levels of these lines is low, polarity indicators (∇) will be used.



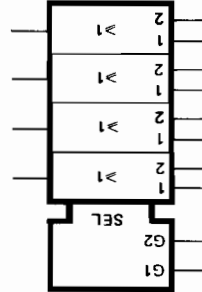
Output selector control block. This symbol is used with a block symbol having multiple outputs to form a decoder. The selection lines enable the output designated 0, 1, ..., n of each block by means of a binary code where S0 is the least-significant digit. If the 1 level of these lines is low, polarity indicators (∇) will be used.



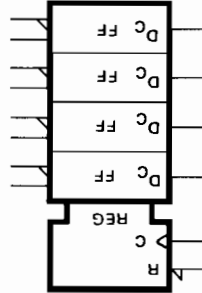
8-32. Complex Logic Devices

8-33. Logic elements can be combined to produce very complex devices that can perform more difficult functions. A control block symbol can be used to simplify understanding of many complex devices. Several examples of complex devices are given here.

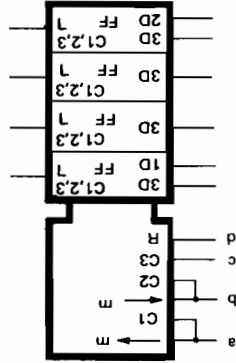
Selector Control Block used to simplify AND portion of a quad AND-OR select gate. When C1 is high, the data presented at the "1" inputs will be gated through. When C2 is high, the data presented at the "2" inputs will be gated through.



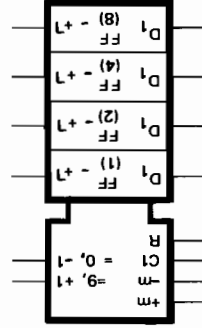
Register control block used to illustrate a quad D-type latch. There is a common active-low reset (R), and a common edge-triggered control input (C). Since there is only one dependency relationship, the controlling input is not numbered and the controlled functions (D) are subscripted with a C.

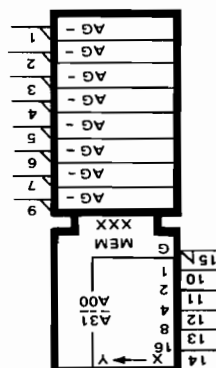


Shift Register Control Block used to show common inputs to a bidirectional shift register. Notice that "←m" means shift the contents to the right or down by "m" units. And "→m" means shift the contents to the left or up by "m" units. Note: If m=1, it may be omitted. Inputs "a" and "b" are each single IC pins that have two functions. Input "a" enables one of the inputs to the top D-type flip-flop (1D), and also shifts the register contents down one unit. Input "b" enables one of the inputs to the bottom flip-flop (2D), and also shifts the register contents up one unit. Input "c" loads all four flip-flops in parallel (3D). Input "d" is a common reset. The output delay indicator is used because these are master-slave flip-flops.



Counter Control Block used to show common inputs to a Presettable Decade Up/Down Counter. Notice that "→m" means count up (increment the count) by "m"; "←m" means count down by "m." Note: If m=1, it may be omitted. Since the D-type flip-flops are master-slave, the output delay indicator is used. The "→9, +1" and "←9, -1" notation defines when the carry and borrow outputs are generated. They also define it, as a decade counter, a binary counter would have carry indicated with "→15, +1." Flip-flop weighting is indicated in parenthesis.





Read Only Memory (ROM) with 32 addresses. Address selection is determined by the five upper inputs which are decoded into 32 possible addresses (A00 through A31) corresponding to the weighting modifiers at the inputs. Input modifier C (pin 15) gates the outputs. Stored data will be read from the selected memory address if C is active (low). The output data pins (1—7 and 9) are active low. The “—” indicator shows the 8 outputs are capable of supplying low outputs only. A high output is usually supplied by a resistor to a “high” voltage.

8-34. TROUBLESHOOTING (FAILURE ANALYSIS)

8-35. Information to help locate a fault or trouble in the 5004A is given in the following material.

8-36. Several troubleshooting aids are permanently built-in the 5004A. The SELF-TEST front panel switch is one. The main assembly (motherboard) NORMAL SERVICE switch is another. The front panel CATE lamp is another. The four-front panel seven-segment digit displays are another. The front panel UNSTABLE SIGNATURE is another.

8-37. The front panel SELF-TEST switch operation is described in Section III of this manual.

8-38. Troubleshooting Flowchart

8-39. Figure 8-1, the troubleshooting flowchart may be used to locate a faulty component. A suggested sequence for troubleshooting is:

- Perform the Operator's Self-Test (see in Section III).
- If the 5004A does not pass the Operators Self-test, perform the steps given in the troubleshooting flowchart (Figure 8-1).

8-40. Major Test Point Signatures

8-41. Table 8-1 lists the signatures for the major test points.

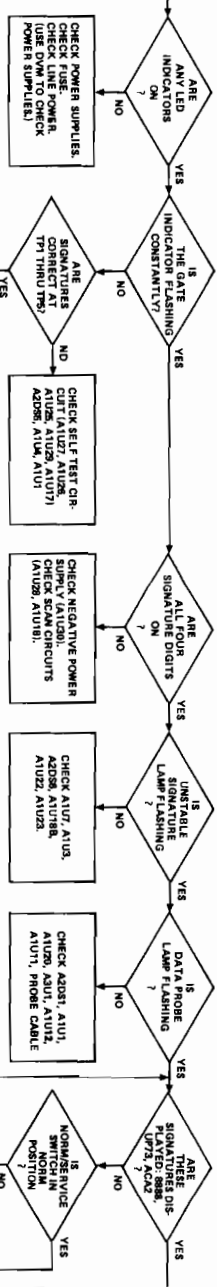
8-42. Troubleshooting Signatures with SELF-TEST and NORMAL/SERVICE Switches

8-43. Table 8-2 is a listing of signatures taken from a correctly operating 5004A with a second correctly operating 5004A. These signatures may be used to locate the cause of a malfunction in a 5004A Signature Analyzer. To take most of the signatures listed requires that the top cover of the 5004A be removed. Refer to the disassembly procedures before attempting to remove the top cover.

WARNING

IF THE 5004A TOP COVER IS REMOVED, DANGEROUS VOLTAGES ARE EXPOSED. ONLY QUALIFIED ELECTRONIC SERVICE TECHNICIANS SHOULD ATTEMPT TO SERVICE THE 5004A WITH COVERS REMOVED.

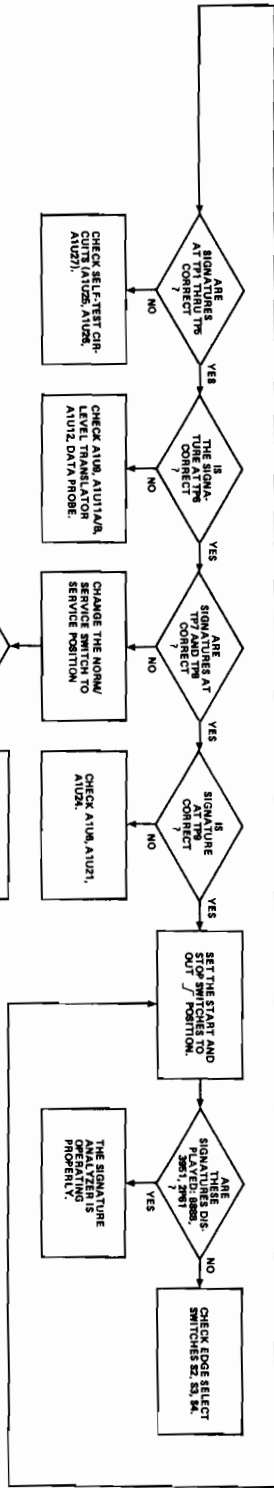
- PRELIMINARY STEPS**
1. SET FRONT PANEL SWITCHES AS FOLLOWS:
TEST - IN, HOLD - OUT
 2. CONNECT TEST PRO START, CORRESPONDING RECP. TACLE ON FRONT PANEL
 3. CONNECT DATA PROBE TIP TACLE ON FRONT PANEL
 4. CONNECT POWER CABLE TO POWER SUPPLY (USE DVM TO CHECK LINE SWITCH ON IML)



SET THE NORM/SERVICE SWITCH TO SERVICE, REFER TO SERVICE SIGNATURE TABLE

IS THE GATE INDICATOR FLASHING?
YES: CHECK A1U2, A1U3, A1U1, A1U2, A1U4

CHECK A1U2, A202, A1U20, A1U21, A1U24, A1U25, CABLE, A1U1, A1U2, A1U3, A1U4



CHECK A1U1, A1U2, A1U3, A1U20, A1U21, A1U24, A1U25, SERVICE SIGNALS

Table 8-1. Troubleshooting Signatures Major Test Points

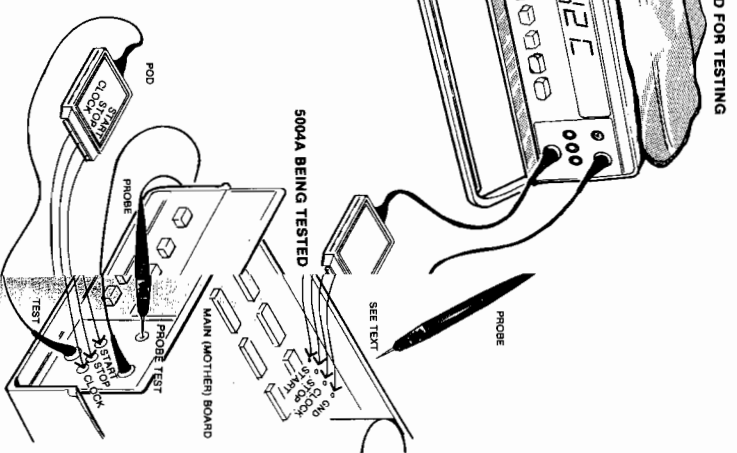
Test Point*	Location	Signature	
		NORMAL	SERVICE
1	U25(11)	FUFU	←
2	U29(1)	54PH	←
3	U29(2)	0155	←
4	U29(3)	HH4b	←
5	U29(4)	HALL	←
6	U9(5)	596F	←
7	U11(8)	U36U	6P6F
8	U7(4), U24(9)	4C4F	125P
9	U24(13), U6(10)	F94H	CFU5

*Test point numbers are shown on the schematic diagram for the 5004A.

Table 8-2. SELF-TEST and NORMAL/SERVICE Signatures

PINS	U1	U2	U3	U4	U5	U6	U7	U8	U9	PIN
1 N	5A22	5A22	TH06	5A22	472A	472A	F577	UCP9	472A	1
2 N	9A43	9A43	H189	9A43	472A	472A	P7A4	P464	472A	2
3 N	A326	A326	0993	472A	472A	0000	P366	3164	7C A7	3
4 N	4646	4646	UCP9	472A	472A	0000	P366	3164	7C A7	4
5 N	1377	1377	UCP9	472A	472A	0000	AC69	472A	0000	5
6 N	4919	4919	62C7	472A	472A	0000	6606	5966	472A	6
7 N	0993	0000	0000	0000	0000	0000	0000	0000	0000	7
8 N	0000	0000	0000	0000	0000	0000	0000	0000	0000	8
9 N	0000	0000	0000	0000	0000	0000	0000	0000	0000	9
10 N	0000	0000	0000	0000	0000	0000	0000	0000	0000	10
11 N	5029	4919	4A25	P466	4A25	5574	0863	4646	4646	11
12 N	3705	4919	5491	H189	5A22	2946	7A33	0166	0166	12
13 N	F61C	4919	5491	H189	9A43	2946	7A33	0166	0166	13
14 N	2946	A326	0166	H189	P366	1467	997P	4596	A446	14
15 N	5A22	472A	472A	472A	472A	472A	472A	472A	472A	15
16 N	472A	472A	472A	472A	472A	472A	472A	472A	472A	16

PIN	U11	U12	U13	U14	U15	U16	U17	U18	U19	U20	PIN
1 N	7C A7	7C A7	7C A7	7C A7	7C A7	7C A7	7C A7	7C A7	7C A7	7C A7	1
2 N	7C A7	7C A7	7C A7	7C A7	7C A7	7C A7	7C A7	7C A7	7C A7	7C A7	2
3 N	7C A7	7C A7	7C A7	7C A7	7C A7	7C A7	7C A7	7C A7	7C A7	7C A7	3
4 N	3164	3164	3164	3164	3164	3164	3164	3164	3164	3164	4
5 N	3164	3164	3164	3164	3164	3164	3164	3164	3164	3164	5
6 N	3164	3164	3164	3164	3164	3164	3164	3164	3164	3164	6
7 N	3164	3164	3164	3164	3164	3164	3164	3164	3164	3164	7
8 N	3164	3164	3164	3164	3164	3164	3164	3164	3164	3164	8
9 N	3164	3164	3164	3164	3164	3164	3164	3164	3164	3164	9
10 N	3164	3164	3164	3164	3164	3164	3164	3164	3164	3164	10
11 N	3164	3164	3164	3164	3164	3164	3164	3164	3164	3164	11
12 N	3164	3164	3164	3164	3164	3164	3164	3164	3164	3164	12
13 N	3164	3164	3164	3164	3164	3164	3164	3164	3164	3164	13
14 N	3164	3164	3164	3164	3164	3164	3164	3164	3164	3164	14
15 N	3164	3164	3164	3164	3164	3164	3164	3164	3164	3164	15
16 N	3164	3164	3164	3164	3164	3164	3164	3164	3164	3164	16



To get the signatures given in this table, set the two 5004A's controls as follows:
 5004A Being Tested
 LINE-OFF; START-OUT; STOP-OUT; HOLD-OUT; SELF-TEST-IN;
 5004A Used to Test
 Same as above except SELF-TEST-OUT
 Make the connections shown between the two 5004A's.

PIN	U21	U22	U23	U24	U25	U26	U27	U28	U29	U30	PIN
1 N	0147	0147	0147	0147	0147	0147	0147	0147	0147	0147	1
2 N	0147	0147	0147	0147	0147	0147	0147	0147	0147	0147	2
3 N	0147	0147	0147	0147	0147	0147	0147	0147	0147	0147	3
4 N	0147	0147	0147	0147	0147	0147	0147	0147	0147	0147	4
5 N	0147	0147	0147	0147	0147	0147	0147	0147	0147	0147	5
6 N	0147	0147	0147	0147	0147	0147	0147	0147	0147	0147	6
7 N	0147	0147	0147	0147	0147	0147	0147	0147	0147	0147	7
8 N	0147	0147	0147	0147	0147	0147	0147	0147	0147	0147	8
9 N	0147	0147	0147	0147	0147	0147	0147	0147	0147	0147	9
10 N	0147	0147	0147	0147	0147	0147	0147	0147	0147	0147	10
11 N	0147	0147	0147	0147	0147	0147	0147	0147	0147	0147	11
12 N	0147	0147	0147	0147	0147	0147	0147	0147	0147	0147	12
13 N	0147	0147	0147	0147	0147	0147	0147	0147	0147	0147	13
14 N	0147	0147	0147	0147	0147	0147	0147	0147	0147	0147	14
15 N	0147	0147	0147	0147	0147	0147	0147	0147	0147	0147	15
16 N	0147	0147	0147	0147	0147	0147	0147	0147	0147	0147	16

Table 8-2. SELF-TEST and NORMAL/SERVICE Signatures

8-44. DISASSEMBLY AND REASSEMBLY PROCEDURES

8-45. To remove the 5004A covers, use the following procedure:

WARNING

WHEN THE COVERS ARE REMOVED FROM THE 5004A, LINE VOLTAGES WHICH ARE DANGEROUS AND MAY CAUSE SERIOUS INJURY WHEN TOUCHED. DO NOT REMOVE THE COVERS UNLESS IT IS NECESSARY.

1. Disconnect the power cable from the rear panel of the 5004A.
2. Turn the 5004A over with the cable case down. Four screws are exposed.
3. On the back panel of the 5004A loosen the two screws at the ends of the heat sink three or four turns (see Figure 8-2).

NOTE

DO NOT loosen the transistor retaining screws (see Figure 8-2).

4. Remove the four screws near the four corners of the cabinet bottom.
5. Hold the top and bottom covers together and turn the 5004A right side up.
6. Carefully lift the top cover off.

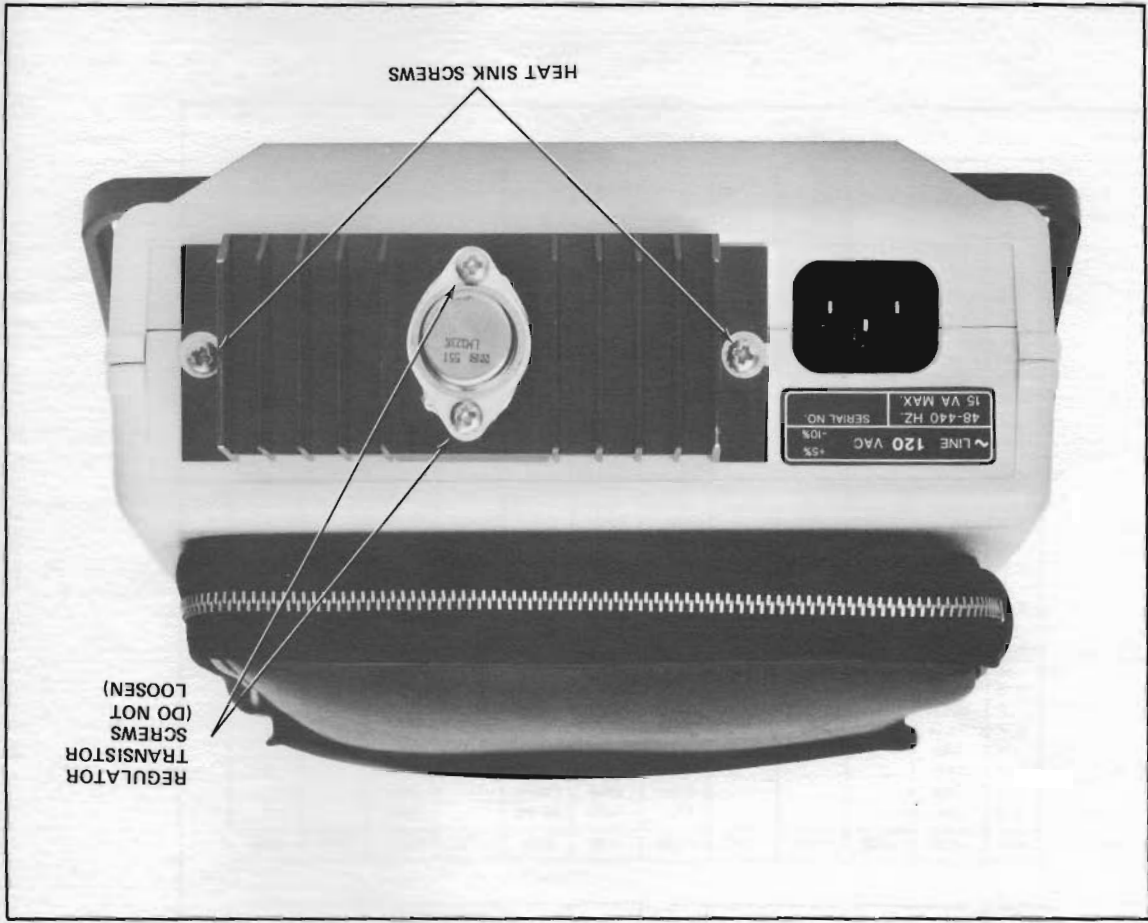


Figure 8-2. Heat Sink Screws Locations

If the heat sink on the rear panel is still holding the cover together, loosen the sink screws a few more turns.

NOTE

BE CAREFUL OF EXPOSED LINE VOLTAGE POINTS.

WARNING

7. If necessary the bottom cover can be removed.
8. To reassemble the 5004A reverse the preceding steps.

8-46. Data Probe Disassembly and Reassembly

- 8-47. To disassemble the data probe, use the following procedure.

1. Disconnect the power cable from the 5004A. Remove the GND wire from the probe.

NOTE

Figure 6-1 shows the mechanical parts of the probe. *Figure 8-7* shows the probe with its covers removed.

2. Remove the probe tip by turning it with fingers counterclockwise.

NOTE

The red window has a projecting stud that fits in the body of the probe near the GND pin (off-set slightly).

3. Carefully pull the red window off the probe tip.

4. Slide the two half covers carefully off the probe printed circuit board.

NOTE

The two body shells interlock to cover the printed circuit board.

5. Reverse the preceding steps to reassemble the data probe.

8-48. Gating Signals Pod Disassembly and Reassembly

- 8-49. To disassemble the gating signals pod, use the following procedure.

1. Disconnect the power cable from the 5004A.

NOTE

Figure 6-1 shows the mechanical parts of the pod. *Figure 8-7* shows the probe with its covers removed.

2. Squeeze the ends of the pod test leads connector and pull the connector off the pod.

3. Remove the four screws from the bottom cover of the pod, and carefully remove the top cover. The bottom cover can also be removed if necessary.

NOTE

The pod cable has a strain protector which fits in a slot in the covers of the pod.

4. Reverse the above procedure to reassemble the pod.

8-50. BLOCK DIAGRAM DESCRIPTION

8-51. In the following paragraphs a description of the 5004A Signature Analyzer is given to match Figure 8-3 the block diagram in this section. A more detailed description of the 5004A is given in the paragraphs following the heading: CIRCUIT THEORY (PRINCIPLES OF OPERATION) (SCHEMATIC DIAGRAM DESCRIPTION).

8-52. A 5004A Signature Analyzer requires four input signals: START, STOP, CLOCK, and DATA. START, CLOCK, and STOP inputs are applied to the 5004A through the GATING SIGNALS POD.

8-53. Data Signal Path. DATA input is through the DATA PROBE. Signals applied to the DATA PROBE are connected to dual paths which trigger at high and low voltage levels respectively. The output of these level detectors is at ECL level and drive a pair of ECL to TTL converters on the main assembly. A logic level detector across the ECL converters provides the drive for the logic level indicator at the data probe tip. The outputs of the ECL converters is translated from a possible three levels (high, bad (middle), and low) to standard high or low levels at the selected clock. (When a bad level appears at the input of the data probe, it is converted to whatever the previous data level was: (either high or low.) Data from the 3-to-2 level converter is applied to the pseudo-random word generator with corresponding gate and clock signals. For each different clocked data stream (series of bits) bracketed by a start and stop signal, a different word (signature) is generated by the word generator. Each signature is sent to the display latches which supply them to the decoder-driver and the signature comparator. The decoder-driver translates the signature to a special-form hexadecimal number which is applied to the display. Each succeeding signature is compared with the preceding signature in the signature comparator which will activate the UNSTABLE SIGNATURE lamp if two succeeding signatures are different. The RESET function for the entire 5004A is part of the DATA probe. RESET is activated by a switch (labeled RESET) on the DATA probe.

8-54. Clock, Start, and Stop Signal Paths

8-55. External CLOCK, START, and STOP signals are applied to the 5004A through the gating signals pod. Input CLOCK, START, and STOP signals are amplified, and connected to operator-controlled edge-select circuits. After edge-selection the CLOCK, START, and STOP signals are combined to form a gating (gate) control signal. (The external CLOCK signal is also buffered and used to time other sections of the 5004A.) The gate signal is presented on the front panel with a GATE indicator lamp. The gate signal is for on-off (start-stop) control of the word generator.

8-56. Scan/Test Oscillator (Internal Clock)

8-57. A .6 kilohertz signals is generated in the 5004A for display scan and test use. The scan signal controls switching the displays on and off (fast enough to be not noticeable) to lower power consumption and reduce the size of drive circuit components. In the SELF-TEST and NORMAL/SERVICE (troubleshooting) modes the internal test signal is used as a substitute for the external clock normally applied to the gating signals pod.

8-58. Self-Test

8-57. Part of the 5004A is a circuit used only for self-test of the signature analyzer. The self-test function is controlled by a front panel switch. In the self-test mode special signatures are generated using the internal test signal frequency divider output (ROM). If there is a defect in the 5004A the self-test signature will not be correct.



Figure 8-3

8-60. Display Scan and Comparator Strobe

8-61. The clock signal is used to time both the display scan and signature comparator strobe circuits. The digit display lamps are enabled less than full-time to conserve power.

NOTE

The NORMAL/SERVICE switch is separate but related to the front panel SELF-TEST switch.

8-62. Service (Troubleshooting) Mode

8-63. On the main assembly of the 5004A a two-position switch, labeled NORMAL/SERVICE, can be used during fault locating (troubleshooting) procedures if the 5004A is not operating correctly.

8-64. Power Supply

8-65. Alternating current line supply (mains) voltage is converted to the two positive and negative regulated direct current voltages required in the 5004A by the power supply circuit.

8-66. CIRCUIT THEORY (PRINCIPLES OF OPERATION)

8-67. The following paragraphs give the circuit theory (principles of operation) for the 5004A Signature Analyzer to explain the schematic diagram. A previous section describes the 5004A at the block diagram level. This BLOCK DIAGRAM DESCRIPTION should be studied and learned before the following paragraphs are studied.

8-68. Purpose of 5004A

8-69. The 5004A Signature Analyzer is designed to be used in testing the correctness of operation of certain complex digital logic electronic instruments or systems. A technique of testing called signature analysis is used with the 5004A and compatible instruments. Refer to the paragraph titled Signature Analysis in Section I for an explanation of signature analysis.

8-70. Schematic Diagram

8-71. The 5004A schematic diagram is presented with the four inputs on the left side, and the flow of signals is generally from the left to the right side where the output indicators are presented. Outputs are four digits (seven-segment LED's) and two single-LED function/condition indicators. Refer to the schematic diagram notes for an explanation of the schematic symbol system used. The ac line power input and dual-voltage (regulated) power supply are on the lower left side of the schematic.

8-72. Gating Signals Pod

8-73. The gating signals pod is the input for the CLOCK, START, and STOP signals to the 5004A. Requirements for these signals are given in Section I. A voltage regulator, U4, for -5.2V on the pod board reduces power dissipation in the main assembly. Amplifier, U1, is used as a voltage follower to provide the 1.4-volt reference level for the three input amplifier-converter. All three input signals are each applied to three separate identical circuits. The input amplifier-converter produces high-speed complementary-output ECL-level signals for the main assembly.

8-74. Edge Selection

8-75. The three ECL-level pulse signals from the pod (START, STOP, and CLOCK) are applied separately to three front-panel switches which may be used to select the polarity of any input signal. Changing the polarity of a signal effectively selects the opposite edge of the input signal as the control for that channel.

8-76. ECL-to-TTL Level Converters

8-77. After the edge select switches the gating signals are applied to four separate ECL-to-TTL level converters. (The CLOCK signal is applied to two separate converters, U12A and B, for two separate paths.) The outputs of the START and STOP level converters are applied to latches which are controlled by the CLOCK signal. The latches outputs are applied to the gate control circuit.

8-78. Gate Control

8-79. The input START and STOP signals are processed in the gate control circuit to produce a definite time window during which data is received by the word generator (described later). Operation of the gate control circuit is described in the following paragraph.

8-80. State Diagram

8-81. Figure 8-4 is a state diagram of the functioning of the gate control circuits. NOTE: Positive-true logic is used. The INITIAL state normally occurs: when the 5004A has power switched on, or when the data probe RESET switch is pressed, or when a STOP and START pulse are received in RUN mode. In the INITIAL state, if START is 0 the state will change to ARMED. In the ARMED state the 5004A is ready to receive a START pulse and proceed to either RUN mode. (Note that if a STOP pulse is received, the state will be intermediate RUN; and to progress to full RUN, STOP must be 0.) From full RUN the state will return to INITIAL if START and STOP pulses are received. If START remains at 0 and a STOP pulse is received, the state returns to ARMED. The HOLD state occurs when the HOLD switch is in and a STOP pulse is received in the full RUN mode. In the HOLD state, the data probe RESET switch must be pressed to return to the INITIAL state. All modes except HOLD have no-change conditions. For example in the ARMED state if the START line remains at 0, the 5004A will not change to RUN. With proper START, STOP, and CLOCK signals the gate control proceeds through the states repetitively. The gate control circuit output starts and stops the word generator, and provides the on-off control of the GATE lamp to show when the START and STOP signals are received and implemented.

8-82. Data Signal Flow

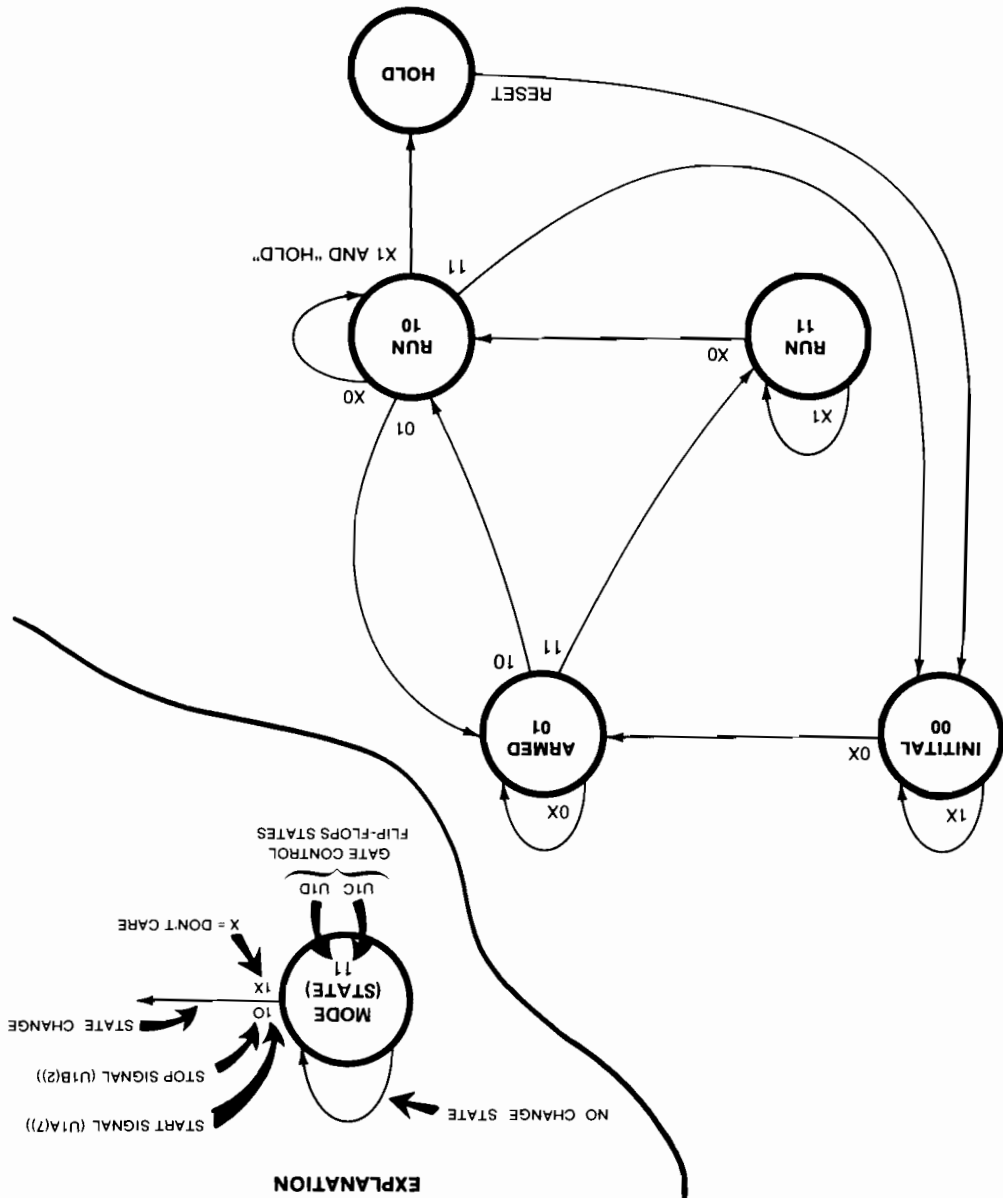
8-83. In normal operation, data signals from the unit being tested are applied to the 5004A high-speed data probe. The data probe (A3) discriminates whether the input TTL level is high or low or bad (middle level). If the input level is high it is detected by U1A, if it is low it is detected by U1B. The input signal is converted to a pair of two-line differential (complementary) ECL signals and sent to the main assembly. At the input to the main assembly the data signal is converted from a pair of two-line (differential) ECL signals to a pair of signals at TTL level. 8-84. The pair of data signals at pins 6 and 12 of U11 (A and B) are applied to the data latch, U9. If the data input signal is a high level or a low level it is clocked out of the data latch on pin 5. If it is a bad (middle) level signal the previous level signal is clocked out of the data latch. (A bad level appears as tow lows at the U9) and K inputs.)

8-85. In the main assembly the data TTL signals at the junction of R37 and R38 are applied to U20, a logic level detector. The detector responds to the combined TTL level (or pulses) of the input signal, and it controls the indication of the logic level indicator lamp, D51, in the data probe. The two TTL data signals are applied to the data latch, J9. Data from U9(5) is applied to U6(5), an "exclusive-OR" gate. This is the input of the pseudo-random word generator.

8-87. The pseudo-random word generator is the central principle of the signature analysis method. A shift register with some outputs fed back to generate a pseudo-random word (signature) output. Input data goes through U6 to shift register U21. From U21(13) the data goes to U24(1 and 2) input. One output from U21 (pin 12) and three outputs from U24 (pins 3, 6, and 13) are fed back to the U6 inputs to combine with the input data and modify the resultant output of the shift registers. The outputs of the two shift registers (U24 and U21) are the unique "signatures."

8-86. Pseudo-Random Word Generator (Data Signal Path Continued)

Figure 8-4. Gate Control State Diagram



8-88. Display Control (Data Signal Path Continued)

8-89. The 16-line signature output of the word generator is applied to the inputs of registers U15, U16, U13, and U14 which drive U19 a memory used as a character decoder. The output of U19 is applied to the four LED seven-segment digits on the display assembly.

8-90. Signature Comparator (UNSTABLE Signature Lamp)

8-91. As each signature is applied to the character decoder, U19, it is also stored in memory U22. When the next signature is received it is compared with the previous signature in U23. If the two signatures are different, U23 outputs a pulse to U7A which is sent to pulse-on the UN-STABLE SIGNATURE lamp on the display assembly, A2. If succeeding signals are identical, U23 does not send a pulse to the lamp. The comparator receives a low-frequency strobe signal from U18B which controls the timing of a store and compare cycle.

8-92. Scan/Test Oscillator

8-93. U28 is a low-frequency (.6 KHz) square wave oscillator. The output of U28 is used for the test circuit and to scan the displays.

8-94. Display Scan

8-95. The front-panel-switched self-test circuit includes U27, U25, U29, and U17. The four-bit counters, U27 and U25 are cycled by a signal from the self-test oscillator, U28, through U26. Outputs of U27 and U26 address memory U29 which supplies START and STOP signals in the self-test mode. All possible states of the gate control circuit are exercised in each self-test cycle to check proper operation. Self-test signals are applied to the inputs of the 5004A to allow all circuits to be tested. Part of the test besides specific signatures is to apply trash to U17 which will exercise all seven segments of each display digit.

8-98. NORMAL/SERVICE Test Switch

8-99. The NORMAL/SERVICE test switch on the main assembly allows all feedback paths in the 5004A to be opened for complete signature analysis testing, with a second 5004A Signature Analyzer. (Refer to the troubleshooting procedures in this section.)

8-100. INPUT SIGNAL TIMING

8-101. Figure 8-5 shows the timing relationship between the input, CLOCK, START, DATA, and STOP signals. The diagram shows that the START signal must transition from low to high before the gate will open, and data in the middle level is accepted as the preceding condition.

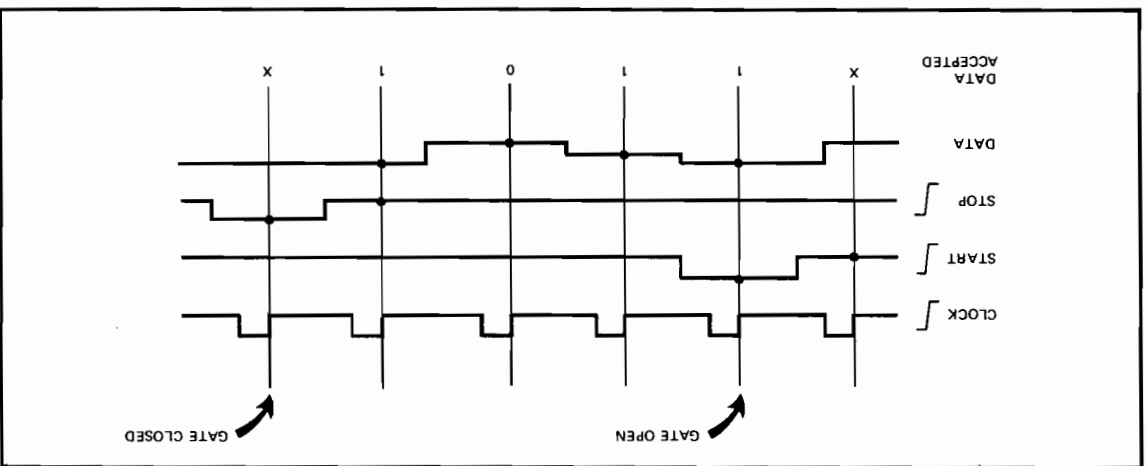


Figure 8-5. Input Signals Timing

SCHEMATIC DIAGRAM NOTES

Resistance in ohms, capacitance in picofarads, inductance in millihenries unless otherwise noted.

Asterisk denotes a factory-selected value. Value shown in typical. Part may be omitted.

Tool-aided adjustment.

○ Manual control.

Encloses front-panel caption.

Encloses rear-panel caption.

Encloses interior or printed-circuit board caption.

Circuit assembly borderline.

Other assembly borderline. Also used to indicate mechanical interconnection (ganging).

Wiper moves toward CW with clockwise rotation of control (as viewed from shaft or knob).

Numbered Test Point.

Measurement aid provided.

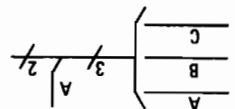
Lettered Test Point.

No measurement aid provided.

A direct conducting connection to the earth, or a conducting connection to a structure that has a similar function (e.g., the frame of an air, sea, or land vehicle).

A conducting connection to a chassis or frame.

Common connections. All like-designated points are connected.



Indicates multiple paths represented by only one line. Letters or names identify individual paths. Numbers indicate number of paths represented by the line.

Integrated Circuit Power Terminals

Unless noted otherwise*, +5 volts is applied to each integrated circuit as given below:

14-Pin Units	Power	16-Pin Units
Pin 14	+5V	Pin 16
Pin 7	Return	Pin 8
Exceptions		
Pin 14	+5V	
Pin 10	Return	

NOTE

Several integrated circuits use the -5.2V power. The -5.2V pins are shown on the schematic diagram.

Figure 8-6. Schematic Diagram Notes

Test point symbols. Stars are numbered or lettered for easy correlation of schematic diagrams, procedures, and locator illustrations. Interconnection information.

Arrow connecting star to measurement point signifies no measuring aid provided.

Star shown connected to circuit signifies measuring aid (metal post, circuit pad, etc.) provided.

Plug-in connection information. Socket designation for A2 assembly.

Number indicates pin of socket (XA2).

J3 not mounted on assembly A2 (or chassis).

Non-plug-in connection information. Solder point named.

REFERENCE DESIGNATION

NO PREFIX	A2 ASSY
J3	A2
Q1	R1

DELETED:

Connector symbols within the borders of circuit assembly signify connections to the assembly which are separate from those made through the integral plug part of the assembly.

Value selected for best operation. Value shown is average or most commonly selected value. Asterisk indicates factory selected component.

Conducting connection to chassis or frame.

Reference designators deleted by circuit changes are listed here.

List of all the reference designations on the diagram.

Assembly reference designator(s).

A2

Figure 8-6. Schematic Diagram Notes (Continued)

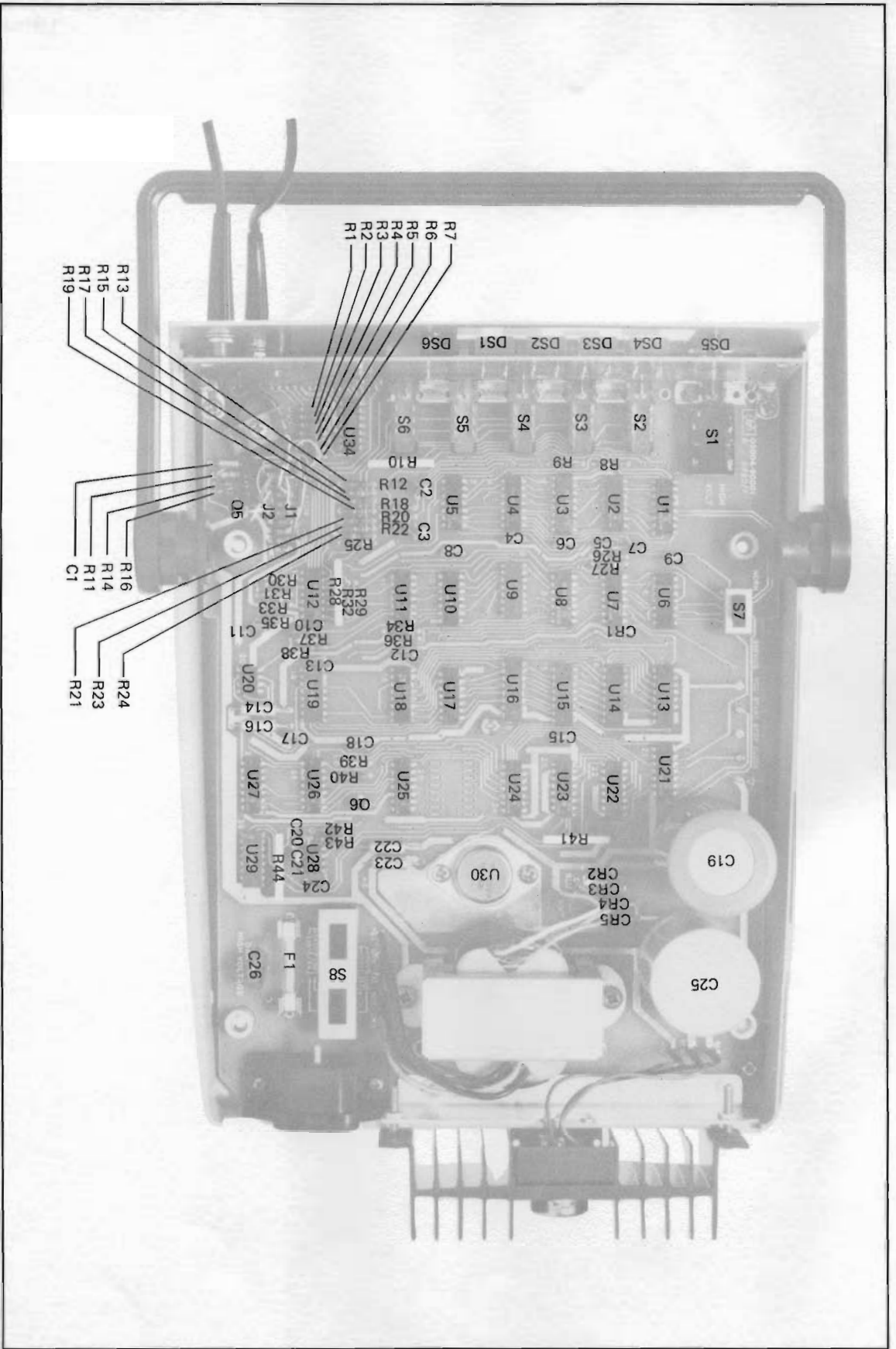
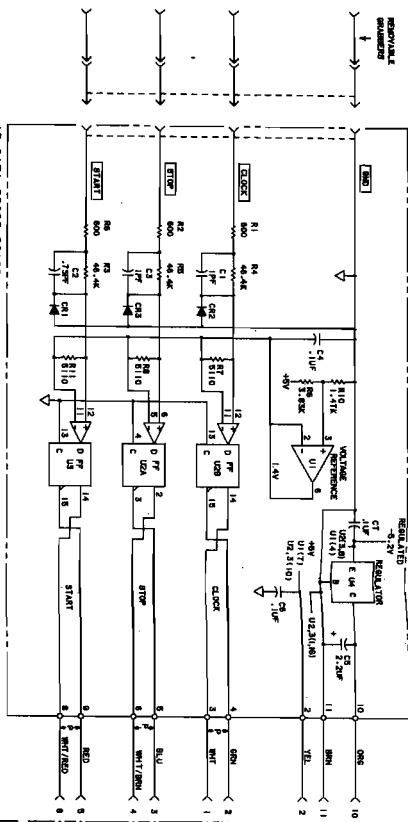
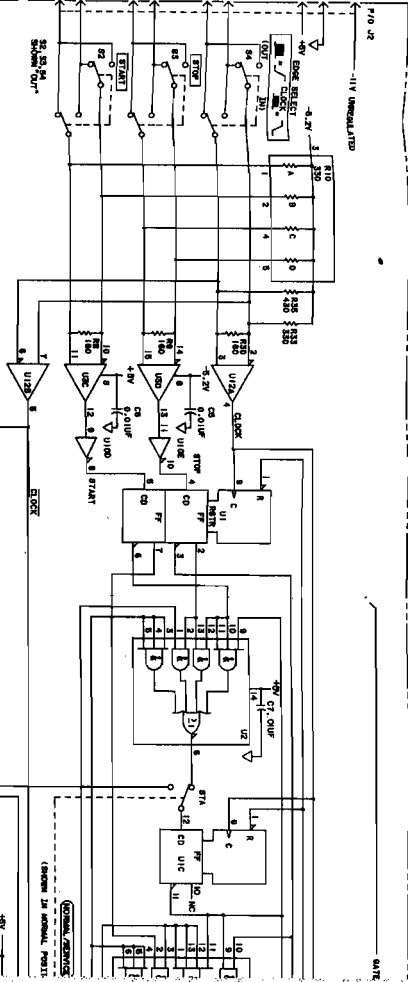


Figure 8-8. Display Board and Main Board (A1) Component Locations

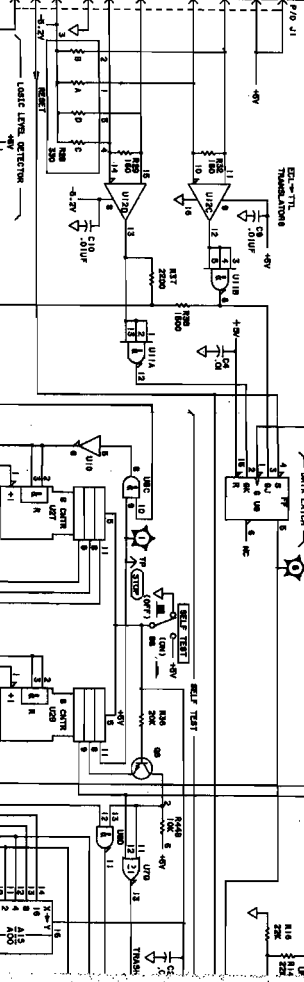
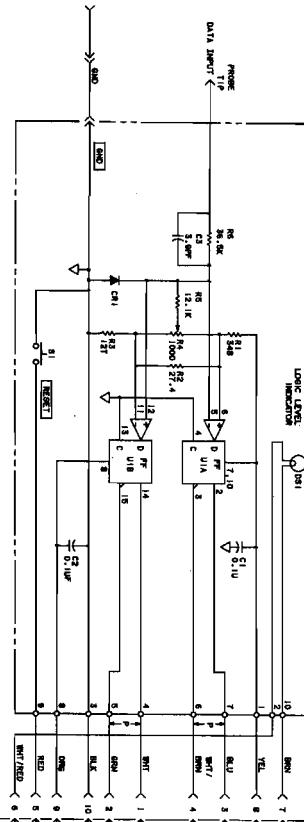
A4 GATING SIGNAL POD BOARD (10004-40004) SERIES 1104



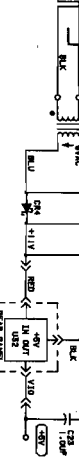
A1 MAIN MOTHER BOARD (10004-40001) SERIES 1104



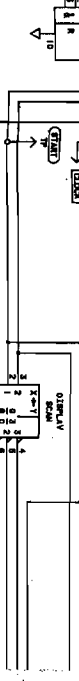
A3 DATA PROBE BOARD (10004-40003) SERIES 1104



1104
SERIES 1104
1104



A1 MAIN MOTHER BOARD (10004-40001) SERIES 1104



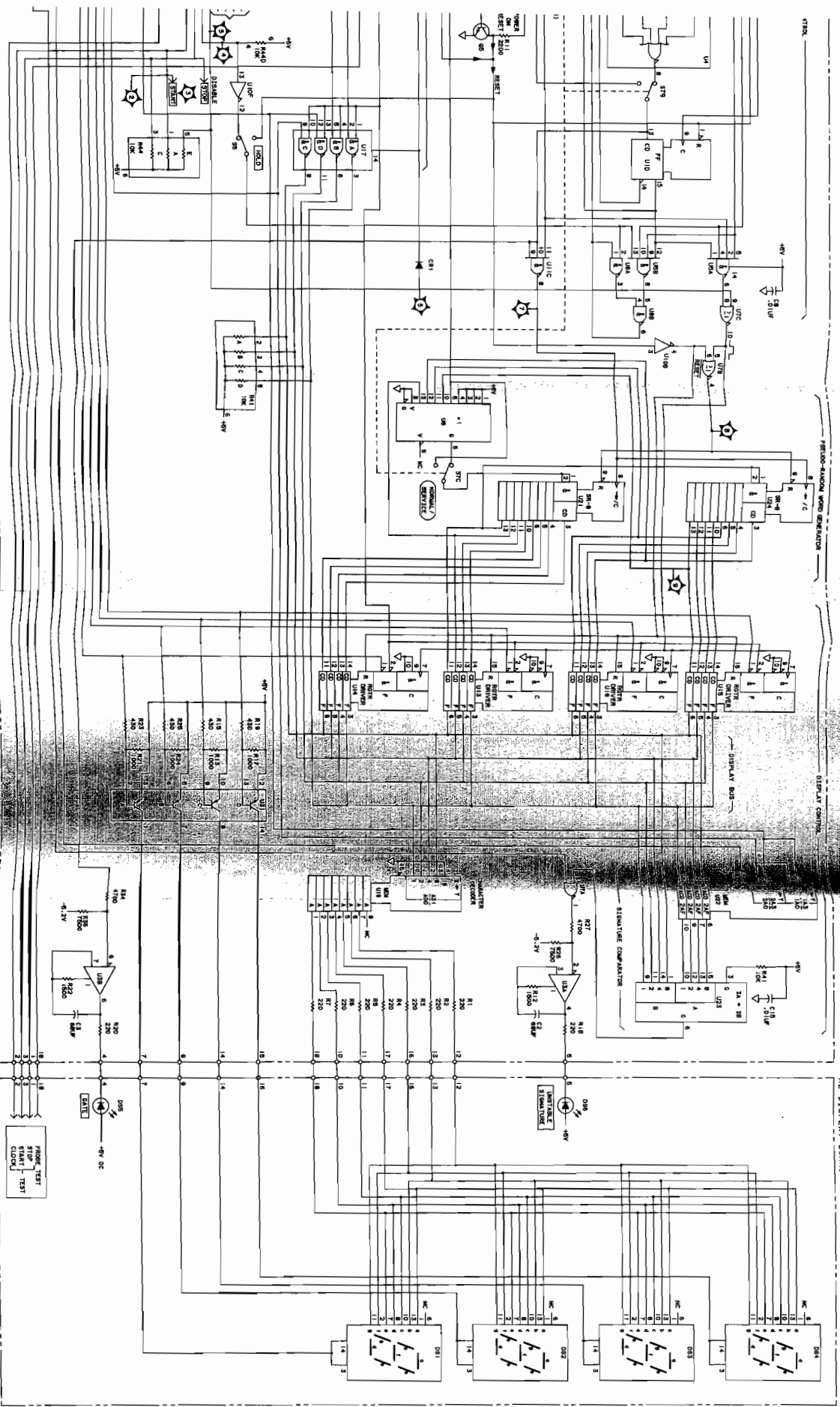


Figure 8-9. Schematic Diagram

